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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/666,220	09/19/2003	Hyun-Jin Cho	C002-D-2	8470
75	90 03/28/2005		EXAMINER	
H.C. Chan			TRAN, MAI HUONG C	
T-RAM, Inc. 100 Headquarters Drive			ART UNIT	PAPER NUMBER
San Jose, CA 95134-1370			2818	

DATE MAILED: 03/28/2005

Please find below and/or attached an Office communication concerning this application or proceeding.





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APPLICATION NO./ CONTROL NO.	FILING DATE	FIRST NAMED INVENTOR / PATENT IN REEXAMINATION		ATTORNEY DOCKET NO.
10/666,22	8			
			EXAMINER	
			ART UNIT	PAPER
				10666220

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Malherry

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner for Patents

IDS 1449 dated 3/18/04 has been considered partially. There are 3 non patent literature documents that are not considered since the copies of these documents are missing. In order for these 3 documents to be considered, please send in copies of these documents.

- Namati, Farid and Plummer, James, A Novel High Density, Low Voltage SRAM Cell with a Vertical NDR Device, VLSI Technology Technical Digest, 6/1998.
- Namati, Farid and Plummer, James, A Novel Thyristor-based SRAM cell (T-RAM) for High-Speed, Low-Voltage, Giga-scale Memories, International Electron Device Meeting Technical Digest, 1999.
- Gribnikov, Z.S., Korobov, V.A., and Mitin, V.V, The Tunnel Diode as a Thyristor Emitter, Solid-State Electronics, Vol. 42, No. 9, 1998, pp. 1761-1763.